AN1510: Neutral-less Dimmer Hardware Design

This application note offers design guidelines for creating a Wi-Fi-enabled, neutral-less dimmer and power supply circuit which is intended to operate in series with a light source using only the live wire. The document aims to address the key technical challenges and to present a practical example solution utilizing the SiWG917 ultra-low power Wi-Fi SoCs and modules.

Note: The design approaches outlined in this document represent viable solutions for neutral-less dimmer applications but are not the only possible implementations. They effectively address the discussed challenges and may be further refined or optimized.

KEY POINTS

- Neutral-less switch solutions
- Forward phase dimming
- Load current path power supply and dimmer hardware architecture
- Power consumption requirements
- Managing power consumption

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1. Introduction

Neutral-less smart switches are designed for homes without a neutral wire, common in older buildings. Using ultra-low-power chips like the SiWG917, these switches draw minimal power directly from the live wire, avoiding flickering in LED lights and enabling near-full brightness. This makes them ideal for easy retrofitting without rewiring.

1.1 Neutral-less Switch Configurations

In neutral-less switch designs, two arrangements are typically considered: The ground current path method and the load current path method.

The ground current method routes the switch's operating current through the protective earth. However, this method is generally non-compliant with safety regulations, which either prohibit such currents during normal operation or impose strict limits. Additionally, unpredictable factors—such as leakage from faulty devices—can compromise reliability. For these reasons, this topology is not considered further in this document.

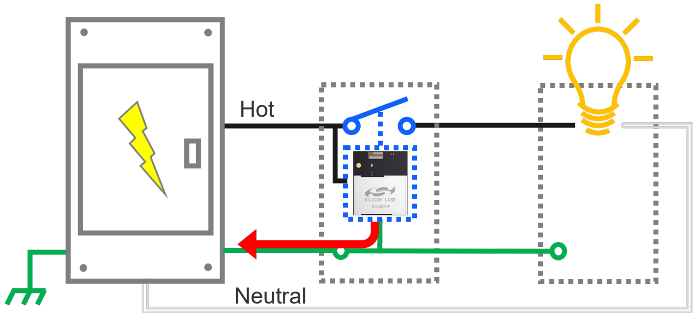

Figure 1.1. Ground Current Path

The Load Current Path method allows the switch to draw ("leak") current through the load (i.e., the light bulb). It is safer and more compliant with regulatory standards. However, it introduces several design challenges:

- Potential visual artifacts in the light output of the bulb
- Tightly constrained
- Increased design complexity

These challenges can be addressed through careful architectural decisions and power management strategies, which are discussed in the following sections.

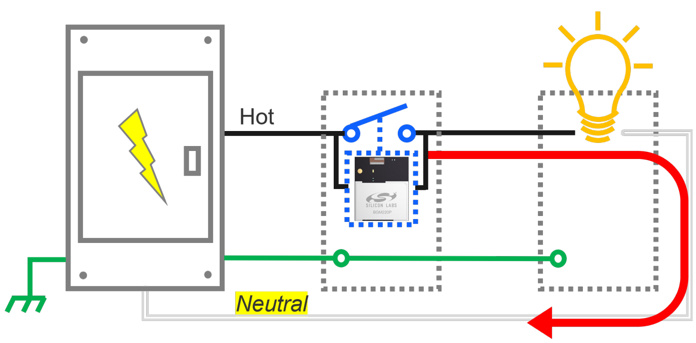

Figure 1.2. Load Current Path

1.2 Light Dimming

Light dimming can be achieved through various techniques. One of the most common and cost-effective methods is phase dimming, which involves switching the load on and off once per AC half-cycle. The brightness is controlled by adjusting the duty cycle of this switching.

The most widely used implementation employs a TRIAC (Triode for Alternating Current) in conjunction with a zero-crossing detector. This setup offers a simple and efficient solution for most dimming applications.

1.2.1 TRIAC Dimming

A TRIAC is a solid-state device used to control AC loads. It is triggered by a short gate pulse and remains conductive as long as the current through it exceeds its holding current. In AC applications, the TRIAC must be re-triggered after each zero crossing to maintain conduction.

In typical forward phase/leading edge dimming applications, power delivery is controlled by delaying the gate trigger pulse after the zero crossing. This delay determines the amount of power delivered to the load. A longer delay results in reduced power and dimmer light output.

Figure 1.3 TRIAC Phase dimming with short gate trigger delay on page 4 and Figure 1.4 TRIAC Phase dimming with long gate trigger delay on page 5 illustrate the effects of short and long gate trigger delays, respectively.

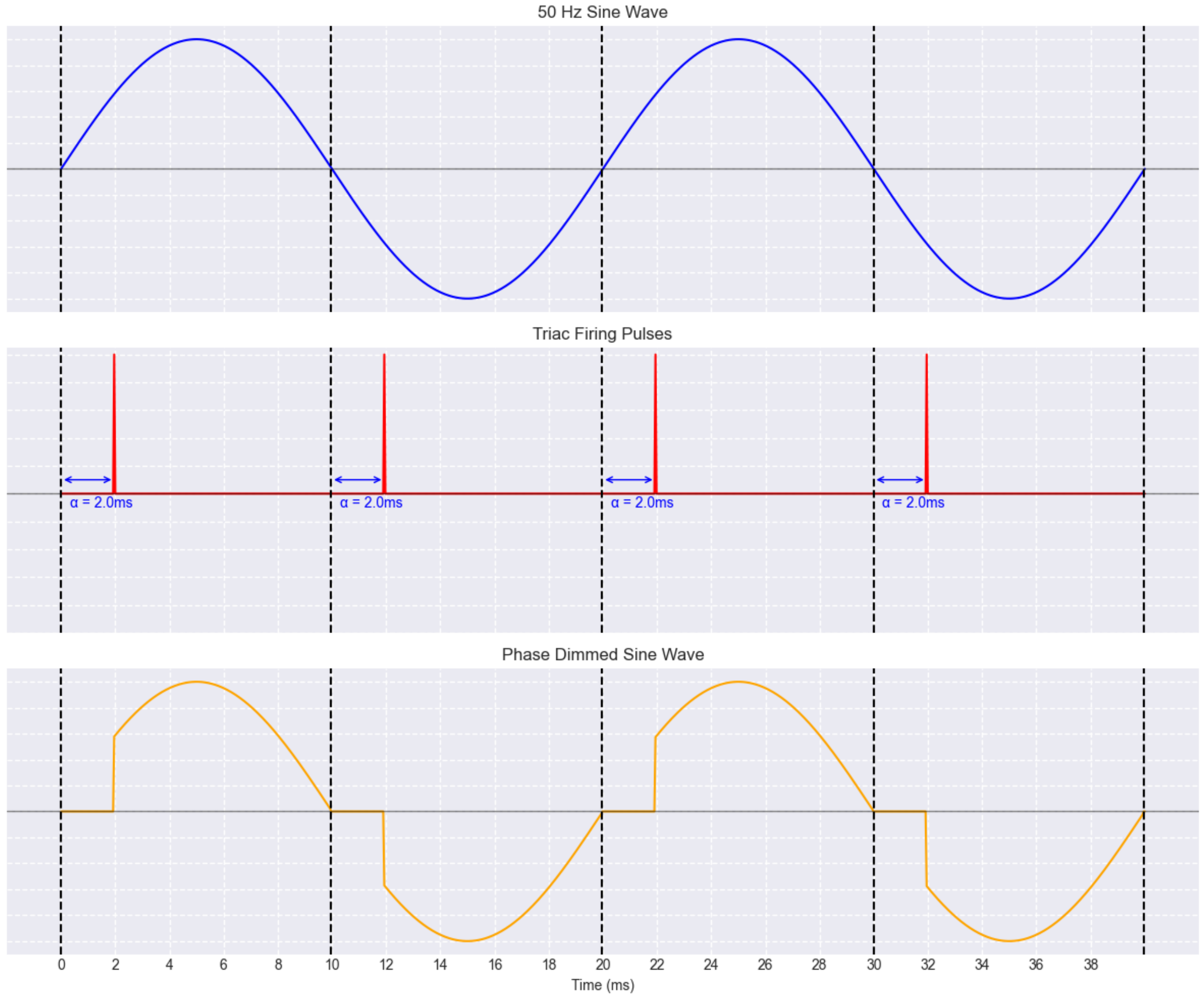

Figure 1.3. TRIAC Phase dimming with short gate trigger delay

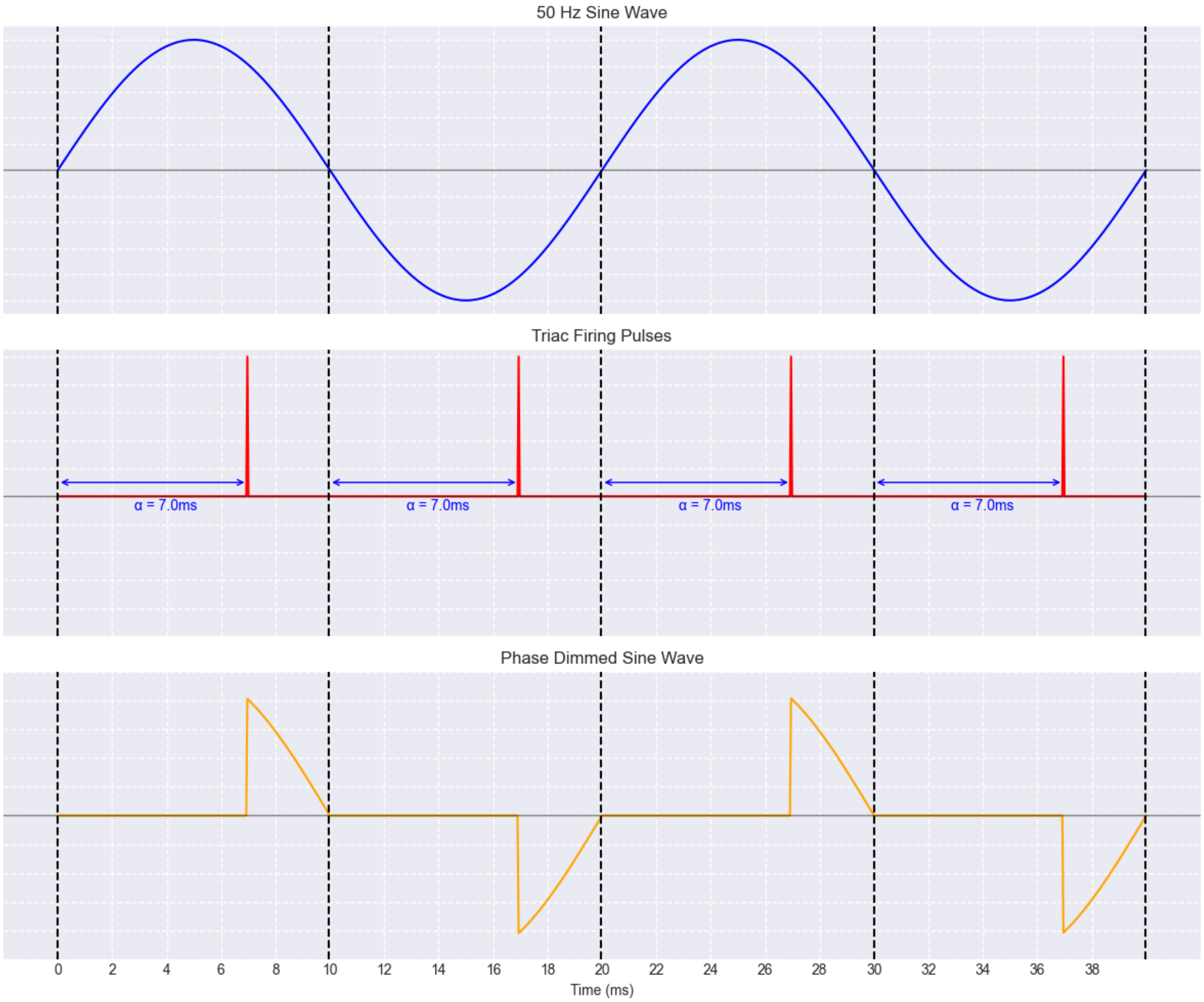

Figure 1.4. TRIAC Phase dimming with long gate trigger delay

1.2.2 Light Bulb Compatibility

Phase dimming introduces a chopped sine wave voltage waveform with rapid transitions, which not all light bulbs can tolerate:

- Incandescent bulbs are highly compatible with phase dimming due to their stable resistance and thermal inertia, which helps smooth out flicker.
- LED bulbs are available in dimmable and non-dimmable variants. Non-dimmable LED bulbs typically cannot handle phase-dimmed waveforms and may flicker or malfunction. Dimmable LED bulbs, designed to emulate resistive loads, are suitable for use with phase dimming.

2. Load Current Path Power Supply and Dimmer Hardware Architecture

In a neutral-less switch application using the load current path, the power supply and dimming circuits must be connected in parallel. This setup ensures enough voltage is available to maintain Wi-Fi connection when the switch is off, while also keeping the current through the load low enough to prevent flicker.

Note: While this document primarily describes only a voltage mode power supply architecture, a dual voltage and current mode power supply could be also implemented which uses current mode in on state to extend the dimming range.

Dimmer Module Functional Components:

- Solid-state relay incorporating a TRIAC
- Low-power zero-crossing detector (ZCD)

Power Supply Module Functional Components:

- Full-wave rectifier
- Step-down converter (e.g., buck or flyback)
- Voltage monitoring circuit (optional)

The following figure illustrates a possible architecture for a neutral-less dimmer power supply and dimming circuitry.

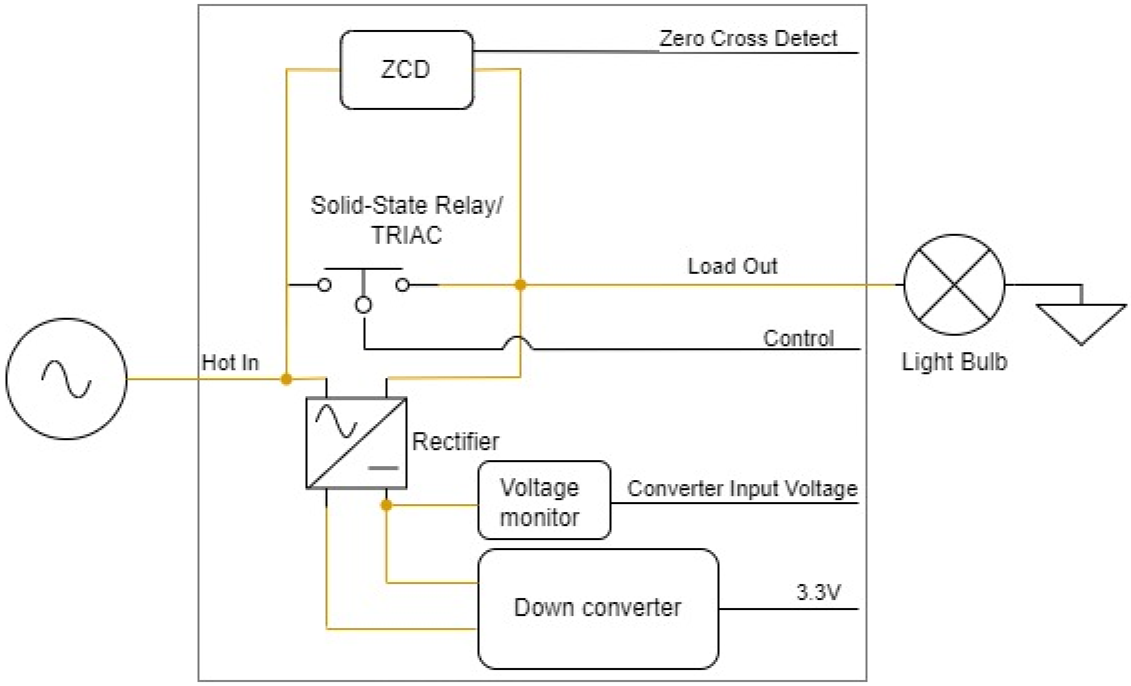

Figure 2.1. Proposed power supply architecture

2.1 Zero Cross Detector

The Zero Cross Detector (ZCD) is critical for synchronizing TRIAC triggering with the AC waveform.

To keep the consumption low on the ZCD, the mains power is fed trough diodes and high-voltage rated resistor in the 100 kΩ-1 MΩ range to divide the voltage down to the comparator input voltage range, and keep the current low. A comparator with a configurable threshold is used to generate the zero cross pulses. The comparison threshold should be non-zero to ensure signal stability.

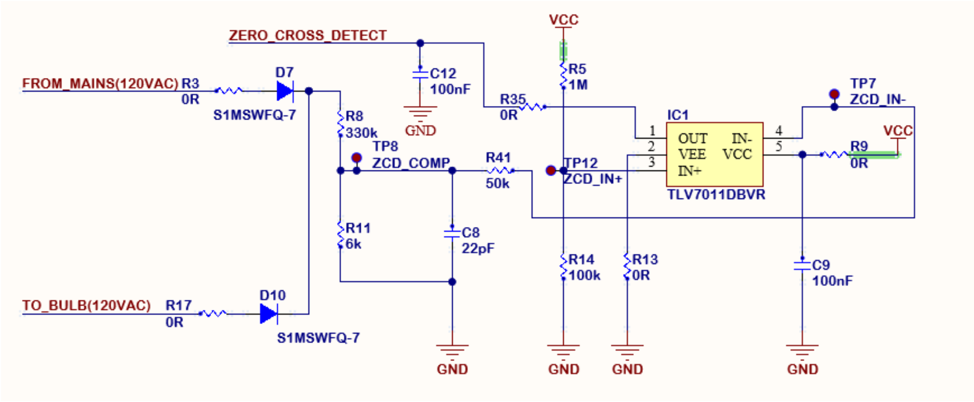

Figure 2.2. Zero Cross Detector schematic

When the bulb is off, the ZCD receives the full rectified waveform and produces consistent ~1 ms pulses at 100/120 Hz. When the bulb is on, the TRIAC shorts the PSU, and the ZCD receives only a portion of the waveform, resulting in a PWM-like signal. The software should trigger only on the falling edge of this signal.

Figure 2.3 ZCD waveform with high lightbulb power on page 7 and Figure 2.4 ZCD waveform with low lightbulb power on page 8 shows ZCD waveforms under different load conditions. The yellow trace is the voltage on the dimmer while the green trace is the ZCD signal.

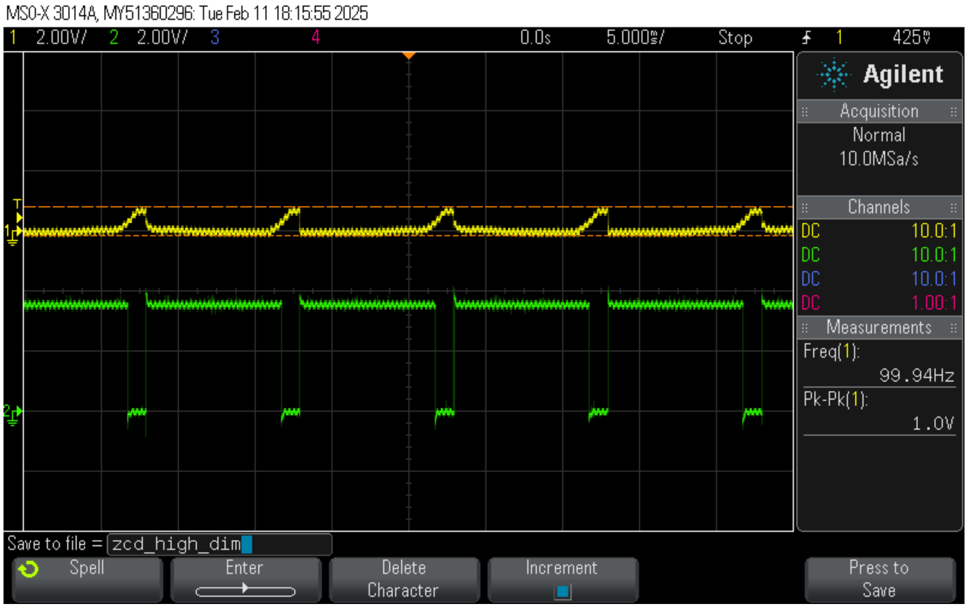

Figure 2.3. ZCD waveform with high lightbulb power

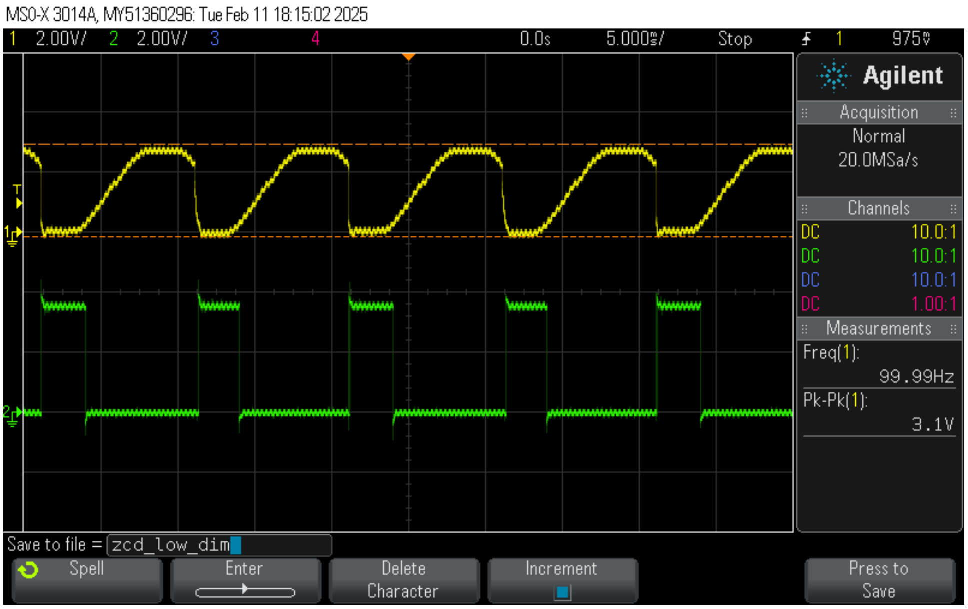

Figure 2.4. ZCD waveform with low lightbulb power

2.2 TRIAC

For optimal performance, use a TRIAC with low holding current, specifically designed for LED dimming. Suitable options include:

- STMicroelectronics T1605G-6I
- Littelfuse Q6016LH1LED

In this design, a Toshiba TLP265J photocoupler was used to trigger the TRIAC. A gate pulse of at least 100 μs was implemented for reliable operation.

Note: This document does not cover detailed TRIAC circuit design (e.g., snubber networks). Refer to manufacturer application notes for guidance.

2.3 Rectifier and Step Down Converter

A full-wave rectifier is essential for charging the input capacitors of the step-down converter. Use low-current diodes (≤1 A) to minimize losses.

Most converter types (buck, flyback, etc.) are compatible with neutral-less designs. Key selection criteria include:

- Low turn-off threshold (preferably <20 V)
- Capability to supply at least 100 mW average output power

The AL17050 buck converter from Diodes Incorporated was used in this design example.

2.4 Voltage Monitor

The voltage monitor tracks the high-voltage buffer capacitors at the converter input for potential interventions (e.g. closing Wi-Fi sockets) to reduce power consumption. Possible implementations are:

- Resistive Divider: Preferred for low power consumption
- Optocoupler: Preferred for galvanic isolation

3. Power Consumption Requirements

To avoid flicker, a commonly used guidance is to limit the power consumption in the low-voltage domain (i.e. the SiWG917 in this case) so that it is <150 mW in every ~100 ms window.

However, during e.g. Wi-Fi transmission and scanning, peak power is typically significantly higher. The power supply must be therefore adequate to accommodate these transients without large input current spikes which could cause flickering or visual artifacts in the light intensity.

3.1 Energy Balance

In the presented architecture, the TRIAC essentially alternates power delivery between the converter and the load. When the TRIAC is off, the converter receives full voltage; when on, the load does.

To ensure sufficient energy for the converter, a minimum gate trigger delay must be enforced This delay depends on the dimmer's energy needs, TRIAC holding current, and ZCD accuracy.

In testing, a 1.3 ms minimum delay was sufficient, resulting in negligible brightness loss (~1 %).

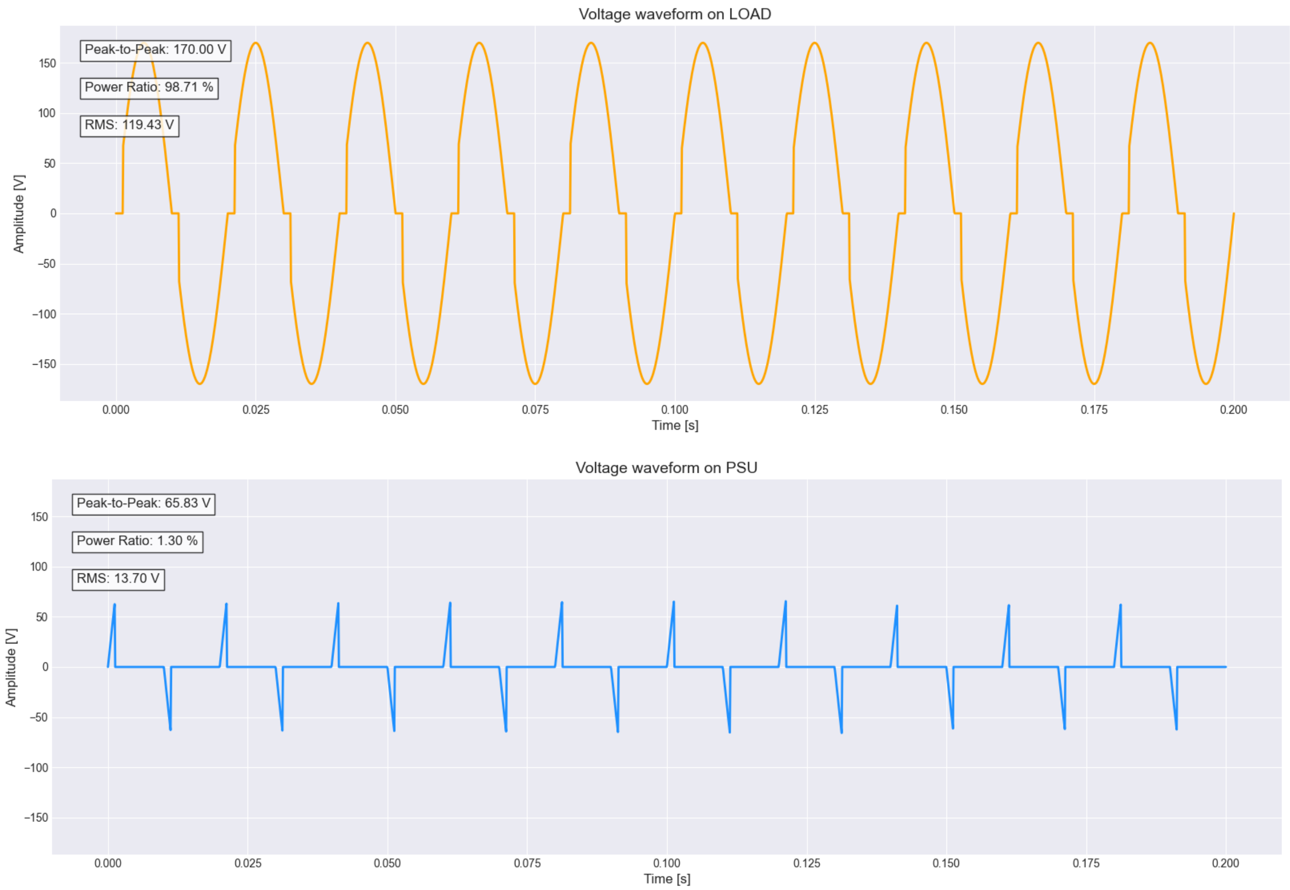

Figure 3.1. Waveforms of the load and power supply voltages with 1.3 ms gate trigger delay

4. Managing the Power Consumption

In terms of available power for the switch, the most critical scenario occurs at max dim level, which corresponds to the minimum allowable TRIAC gate trigger delay. In this state, the high-voltage input capacitors ($V_{HV\text{-}caps}$) are at their lowest charge level, limiting the available energy.

During high-power events such as Wi-Fi transmission, the power supply must maintain stable operation:

- The output voltage (V_{PSU}) must remain high enough to prevent brown-out
- The input voltage ($V_{HV\text{-}caps}$) must stay above the converter's turn-off threshold (Vturn-off)

The down converter's output buffer capacitors (V_{PSU}) cannot go below the SiWG917 lowest possible supply voltage, ($V_{PSU\text{-}low}$), which is 2.97 Volts (check datasheet for the most up-to-date value).

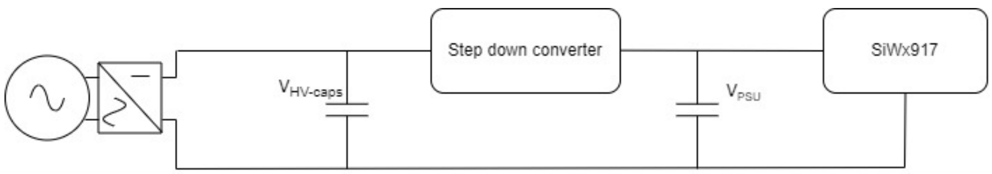

Figure 4.1. Power supply capacitor positions

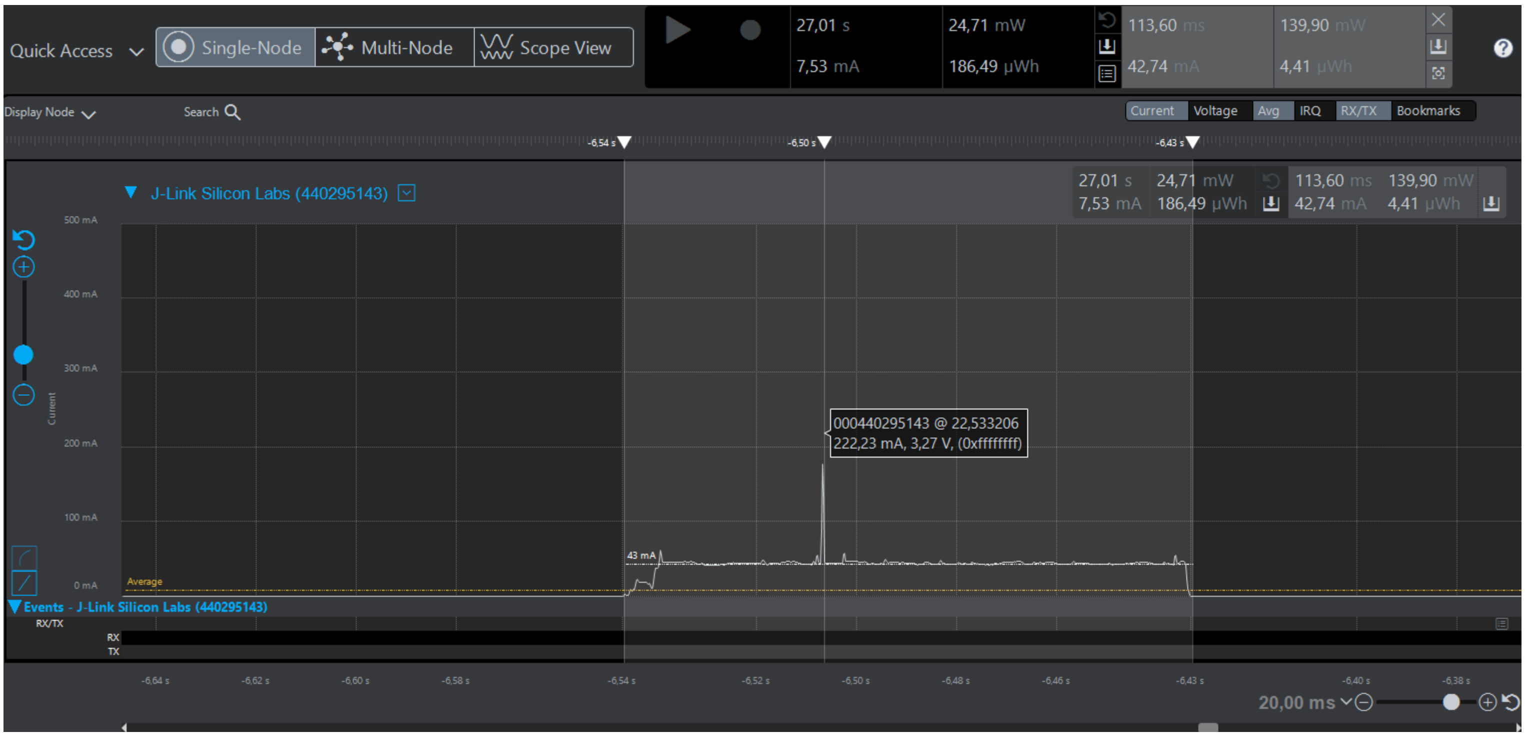

Figure 4.2. SiWG917 current consumption with 20 dBm TX transmit event

To validate the power supply circuit, it should be tested under the system worst case conditions (e.g. max. brightness + Wi-Fi transmission) or using a DC programmable load mimicking these conditions. Recommended parameters to measure/test:

- $V_{HV\text{-}caps}$ where V_{PSU} >= $V_{PSU\text{-}low}$, immediately after transmit, this should be $V_{HV\text{-}caps\text{-}min}$
- $V_{turn\text{-}off}$
- Minimum trigger delay, to accomodate $V_{HV\text{-}caps\text{-}min}$
- Maximum trigger delay, without flicker

Ideally, the trigger delay boundaries ensure robust operation, the converter's voltage levels can be monitored and some Software control strategies could be implemented to prevent brown-out, such as:

- Monitor $V_{HV\text{-}caps}$ and increase the TRIAC delay if voltage drops below Vturn-off
- Before Wi-Fi transmission, ensure $V_{HV\text{-}caps} \geq V_{HV\text{-}caps\text{-}min}$

- Adjust the the minimum gate trigger delay to maintain $V_{HV\text{-}caps}$ at or above $V_{HV\text{-}caps\text{-}min}$

Finally, during configuration (e.g., 4-way handshake), power consumption may spike. To mitigate this, the light bulb may be also dimmed to a low (but non-zero) brightness level to maximize energy recovery.

5. Revision History

Revision 1.0

June, 2025

Initial release.

Simplicity Studio

One-click access to MCU and wireless tools, documentation, software, source code libraries & more. Available for Windows, Mac and Linux!

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